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Effect of lattice mismatch on gate lag in high quality InAlN/AlN/GaN HFET structures

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Grown lattice matched to GaN, InAlN-based heterojunction field effect transistors (HFETs) are promising due to the relatively large band discontinuity at the interface and lack of misfit strain. Despite the recent progress in the growth, there still exists some questions as to the true lattice matching condition of InAlN to GaN due to discrepancies in the value of the lattice parameters of the InN binary, as well as the literature value of the InAlN bowing parameters. In order to address this, we used the gate lag as a supplementary measurement to verify lattice matching to the underlying GaN, as strain-free layers would not have piezoelectric charge at the surface, which would be one source of lag. We observe very low lag for a nearly lattice matched barrier, and a marked increase as the composition deviates from the lattice matched condition. Additionally, FETs fabricated on a nearly matched layer boast a maximum drain current of over 1.5 and ~2.0 A/mm and transconductances of ~275 and ~300 mS/mm at DC and in pulsed modes, respectively, and a cutoff frequency of 15.9 GHz (an fT*LG product of 10.3) for a gate length of 0.65 μm.

1 Introduction GaN-based heterojunction field effect transistors (HFETs) exhibit very respectable performance in the high frequency-high power arena [1]. One opportunity to further enhance the performance of HFETs is through replacement of the AlGaN barrier layer with Al-rich InAlN with relatively large bandgap [2–8]. The power performance is proverbially thought to improve through the ensuing increased carrier density due to the relatively large difference in polarization at the interface where the 2-dimensional electron gas (2DEG) resides [9]. For example, a typical $Al_{0.3}Ga_{0.7}N$/GaN interface would have a difference in spontaneous polarization of 0.017 C/m^2 while an $In_{0.16}Al_{0.84}N$/GaN interface would have 0.048 C/m^2, according to the recommended polarization values given by Ref. [10]. Fortuitously, this barrier boasts a larger band offset with respect to GaN, (as compared to a typical $Al_{0.3}Ga_{0.7}N$ barrier) which results in better carrier confinement and a deeper quantum well [2, 3]. An additional benefit of the InAlN barrier layer over the more mature AlGaN one is that one can more easily scale the thickness of the barrier [11], imperative to avoid short channel effects when scaling the gate length, without the reduction of the sheet density [9]. From a reliability point of view, the pairing of InAlN with GaN is attractive because these materials can be lattice matched, circumventing strain related maladies that plague the AlGaN/GaN system [12, 13]. Additionally, the strain-free InAlN barrier is expected to exhibit reduced gate lag [14, 15] since the lag has been attributed to the charging and discharging of traps coupled with instable (polarization) charges on the surface of the devices [16–19]. The difficulty, however, lies in the growth of the InAlN barrier layer. In-containing compounds need to be grown at relatively low temperatures as compared to AlN or else suffer from In segregation, reduced incorporation of In, and In-clusters [9]. Additionally, the lattice matching condition is not precisely known as there is some scatter in the literature in the values of the lattice parameters of the binaries, as well as uncertainty in the amount of deviation from Vegard's law (bowing). Furthermore, initial reports of InAlN/GaN heterostrucutres suffered from very low mobilites which can likely be attributed to the large degree of alloy scattering that occurs at this interface not only due to the high alloy potential of InAlN (if one were to use the popular estimation of the difference in conduction band offsets between the constitutive binary compounds, clearly InN-AlN would be larger than AlN-GaN), but also due to the deeper well effectively moving the centeroid of the 2DEG wavefunction closer to the InAlN/GaN interface. Despite this, with the inclusion of an AlN

spacer layer to improve the 2DEG mobility [5, 20], respectable performances have been demonstrated [21–23]. In this manuscript, we report on the effect of the barrier layer composition on the gate lag suffered by these devices and find that the lag increases as the layers move further from lattice matching. Additionally, we find that though the gate lag is not attributable to the amount of gate leakage, it is correlated to the rate of change of the gate leakage current, suggesting that as gate leakage paths open up as bias is changing, traps that are responsible for gate lag become activated and can contribute to the lag.

2 Experiment Three InAlN/AlN/GaN HFET structures were grown on sapphire substrates in a low-pressure custom-designed Organo-Metallic Vapor Phase Epitaxy (OMVPE) system. Trimethylgallium (TMGa), trimethylaluminum (TMAl), trimethylindium (TMIn), and ammonia were used as the Ga, Al, In, and N sources, respectively. First an initiation layer of AlN (250 nm) was grown at ~1030 °C at a chamber pressure of 30 torr, followed by 3.0 μm of undoped GaN deposited at ~1000 °C at 200 torr. Next, an optimized AlN spacer layer was grown at 1000 °C with a thickness of 0.8–1 nm, which was determined from X-ray diffraction (XRD) data from a superlattice calibration structure grown under identical conditions. Next, the temperature was ramped down and the carrier gas switched from H_2 to N_2 for 20 nm of InAlN growth. The composition of the InAlN barrier was controlled by varying the temperature between 775 and 800 °C. Finally, the temperature was ramped up to ~900 °C for the deposition of a ~2 nm thick GaN cap layer. In the following, we will call the layer with the InAlN barrier grown at highest temperature (and thus the lowest incorporation of In) "A", next highest temperature will be "B", and lowest temperature (with the highest In composition) will be referred to as "C".

3 Results and discussion

3.1 Structural To determine the residual strain in the underlying GaN buffer layer, photoluminescence at 10 K was measured and compared to that from a 250 μm thick layer of freestanding bulk hydride vapor phase epitaxy (HVPE)-grown GaN. The energy of the free A-exciton (FXA) transition was found to be blue shifted by 21.8 ± 1 meV, which corresponds to a strain of 0.227 ± 0.009% in the *a*-axis or 0.11 ± 0.05% in the *c*-axis of GaN grown on sapphire, relative to the bulk [9]. Using Vurgaftman and Meyer's "recommended" values [10] of the bulk *a* lattice parameters of 3.189, 3.112, and 3.545 Å for the GaN, AlN, and InN binaries, respectively, and considering the bowing parameter of the *a* lattice constant of InAlN to be –0.01 [24], this amount of strain translates into *a* lattice matched composition (matching the *a* parameter) of $x = 15.8\%$ for $In_xAl_{1-x}N$ barrier layers (we have assumed that the bulk layer has the aforementioned lattice parameter and is additionally strain free). If one were to disregard the strain present in the GaN after growth on sapphire substrates, using the above-mentioned values for the lattice constants of the binaries, one would expect lattice matching at $x = 17.4\%$. Therefore, it is clear that the strain in the underlying layer is important to consider when attempting to ascertain the composition required to match InAlN to the GaN layer in hand. Furthermore, the picture is clouded some when one considers the uncertainty in the lattice parameters of the binaries, particularly InN, as well as the uncertainty in the bowing parameters. For example, taking the values of the *a* parameters of the binaries to be 3.185, 3.111, and 3.5377 Å for GaN, AlN, and InN as done by Lorenz et al. [24], one obtains the lattice matched condition to be 17.0 and 15.3% on bulk GaN and strained GaN, respectively.

In order to determine the composition of the three layers under investigation, we measured the shift in the angle of reflection between the GaN peak and the InAlN peak in an XRD 2θ-ω scan, which allows one to determine the InAlN *c* parameter through the Bragg relation. This value was then used to estimate the composition of the InAlN layer assuming a bowing parameter of the *c* lattice parameter of −0.075 [24]. Of course, this method first assumes that the layers are fully pseudomorphic and free of strain; however, in reality only a structure that is in fact lattice matched is free of strain. Also, thickness interference fringes were clearly resolved from XRD, from which a barrier thickness of ~20 nm for each of the layers was also determined. By using the *c* lattice parameters given by Vurgaftman and Meyer [10] (5.185, 4.982, and 5.703 for GaN, AlN, and InN, respectively), we estimated the In composition of the InAlN barriers for samples A, B, and C to be 14.8%, 16.6%, and 21.7%, respectively. If we had used the values given by Lorenz et al. [24] (taking the *c* parameters to be 5.188, 4.98, and 5.7037) we would have found layers A, B, and C to have compositions of 15.4%, 17.2%, and 22.0%, respectively. As such we consider sample "A" to be closest to being lattice matched, sample "B" to be nearly lattice matched, and sample "C" to be lattice mismatched. If we changed the bowing parameters of the *a* and *c* lattice constants to those reported in Ref. [25], we would have the lattice matching conditions (using lattice parameters from Ref. [10]) of 20.1 and 18.3% (without and with the underlying strain of the GaN), with our layers having compositions of 13.5, 15.2, and 19.9%, thus sample C would be closest to being lattice matched. Considering our results as well as the grazing incidence refraction (GID) results reported in Ref. [24] which showed contradictory behavior when the bowing parameters of Ref. [25] were used in conjunction with their experimental data, our data are consistent with the bowing parameters of Ref. [24].

3.2 Electrical Following structural characterization and evaluation of the layers, variable temperature Hall measurements were performed using a van-der-Pauw geometry. At room temperature, respectable mobility values of 1020, 1050, and 1350 cm^2/Vs with corresponding sheet carrier densities of 2.95×10^{13}, 2.6×10^{13}, and 1.5×10^{13} for samples A, B, and C, respectively, were measured. These mobility values are comparable with the highest reported

thus far in the literature for the sheet densities over 2.5×10^{13} [5, 6]. The low temperature mobility is expected to be much more sensitive to electron concentration as well as to defects and imperfections in the crystal, and as such we can use it to compare the quality of similar structures. Shown in Fig. 1(a) is the mobility versus sheet density at 77 K for our layers with high sheet carrier density (samples A and B) as well as other nearly lattice matched, Al-rich InAlN layers, and an AlN/GaN layer from the literature for comparison. Figure 1(b) shows for the same set of samples the true figure of merit for the 2DEG transport, the mobility-sheet carrier density product, which is directly related to the sheet resistance of the layer.

We can attribute the high mobility and high mobility-density product at low temperature to the high quality of our InAlN/AlN/GaN layers. As we expect the centroid of the 2DEG wavefunction to approach the interface as the density is increased, the mobility of the high density 2DEG will be affected by alloy scattering and interface roughness scattering at low temperatures. The alloy scattering is effectively suppressed as mentioned in Ref. [26] which reported a self-consistent calculation resulting in a penetration depth of the 2DEG of only ~0.7 nm when a 1 nm AlN spacer layer is employed. Therefore, the wavefunction only penetrates the AlN spacer and alloy scattering should be negligible. Of course, the effective band offset changes with the composition of the barrier layer and would be reduced as the In composition increases, increasing the electron wavefunction penetration slightly. In any case, the alloy scattering is expected to be low when an AlN spacer layer is employed. As such, the interface roughness may dominate the low temperature mobility, as reported recently by Tülek et al. [7]. We attribute our low interface roughness to a smooth growth front, as well as our optimization of the thickness and deposition pressure of the high temperature AlN spacer layer [20].

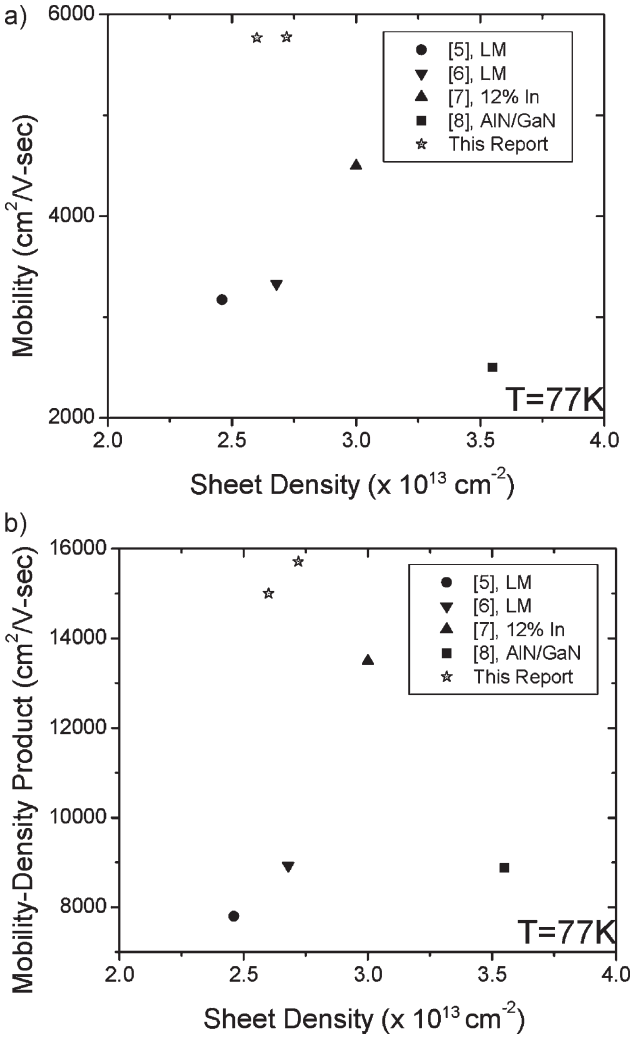

Figure 1 (a) Mobility and (b) mobility-density product versus sheet density at 77 K for the (InAlN)/AlN/GaN heterostructures investigated in this report as well as data from the literature for comparison.

3.3 HFET The field effect transistors were fabricated using Ti/Al/Ni/Au Ohmic contacts followed by etched mesa isolation in a SAMCO inductively coupled plasma (ICP) etch tool using a Cl-based chemistry. Finally, gate electrodes were fabricated using a standard liftoff procedure using Pt/Au (30/50 nm). We found that Pt contacts exhibit about an order of magnitude lower gate leakage current as compared to Ni-based contacts, similar to the results reported in Ref. [27]. The devices were not passivated. The fabricated transistors demonstrated high peak drain currents as well as high transconductances as illustrated in Fig. 2. For devices on the sample A, with lowest In and most closely lattice matched, the peak drain current density is over 1.5 A/mm at DC (about 2.0 A/mm pulsed mode) at a forward gate bias of +2 V for gate lengths of 1.2 μm and source–drain separations of 3.5 μm. The pulsed measurements are taken from quiescent bias point of $V_G = 0$, $V_D = 0$, using a pulse width of 1 μs and a 0.1% duty cycle. The reduction in drain current at DC as compared to pulsed mode can be ascribed to the self-heating effect which is exacerbated by the low thermal conductivity of the sapphire substrate, and is particularly evident at high drain current levels. The measured peak transconductances were about 275 mS/mm at DC and over 300 mS/mm under pulsed mode, for a drain voltage of 7 V. The data in Fig. 2 are from a device with a gate width of 45 μm, but devices with gate widths of 145 μm exhibited similar performance. Additionally, small signal scattering parameter measurements on a device with a gate length of 0.65 μm demonstrated a cutoff frequency of 15.9 GHz (for a $f_T{}^*L_G$ product of 10.3) and a maximum frequency of oscillation of 19.1 GHz. The S-parameter measurements were taken at CW at a bias of $V_G = -7$, $V_D = 7$ V. The maximum drain current density in devices further from the lattice matched condition with higher In compositions (samples "B" and "C") decreased to about 1.4 A/mm and 0.9 A/mm at DC and about 1.9 A/mm and 1.2 A/mm under pulsed mode, respectively, with +2 V applied to the gate.

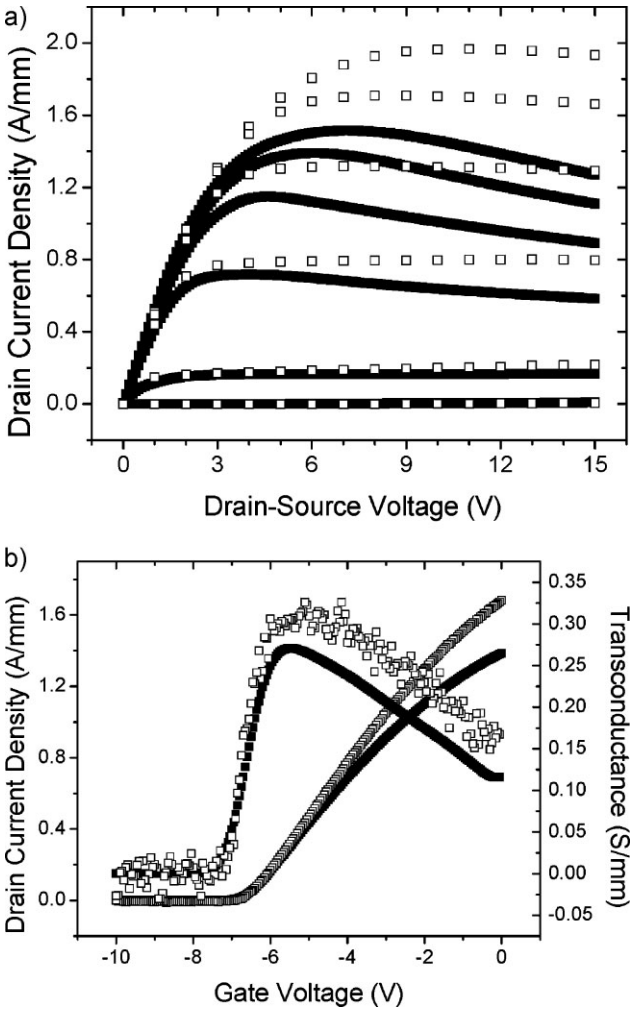

Figure 2 (a) DC (solid squares) and pulsed (open squares) I_D versus V_{DS} curves for the InAlN/AlN/GaN structure that is closest to being lattice matched, "A". The peak drain current is over 1.5 A/mm for a gate voltage of +2 V at DC and about 2.0 A/mm for a pulse width and period of 1 μs and 1 ms, respectively. The difference stems from the low thermal conductivity of the sapphire substrate which results in self-heating effects suppressing the drain current during the DC measurement. The gate voltage steps are from +2 V (top) to −8 V in −2 V steps. (b) I_D versus V_G curve demonstrating a peak transconductance of ∼275 mS/mm at DC (solid squares) and over 300 mS/mm using a 1 μs pulse (open squares). The drain voltage is 7 V.

In an effort to understand the effect of lattice mismatch on the gate lag, pulsed measurements with 1 μs long pulses and 1 msec period under various quiescent voltages were performed. The results are shown in Fig. 3 for a device on the slightly mismatched sample B, which was chosen for display due to its moderate amount of lag. Pulsing from a quiescent voltage representing the open channel state ($V_G = V_D = 0$) results in the highest current values. This is considered the "baseline" to which further pulsing will be compared in order to quantify the degree of gate lag. Pulsing from a quiescent voltage under which the channel is about halfway

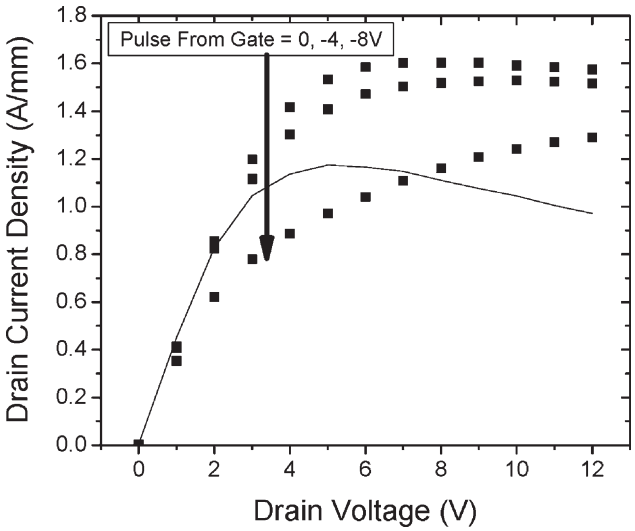

Figure 3 DC (solid line) and pulsed IV (solid squares) demonstrating the gate lag effect in the sample which is slightly lattice mismatched, "B". The pulses (1 μs) are from quiescent voltages $V_D = 0$ V, $V_G = 0, -4, -8$ (pinchoff).

pinched off ($V_D = 0$, $V_G = -4$ V) results in an IV curve that is still higher than DC (solid line). One might therefore argue this layer to thus be lag free, as is commonly done in the reported data [14, 15] but in fact, comparison should be made not to DC but to the "baseline" (i.e., pulsing from the open channel ($V_G = V_D = 0$) state). In this case, it is clear that some gate lag is still present. Pulsing from the full pinch-off condition ($V_D = 0$, $V_G = -8$ V) results in a moderate gate lag as the drain current falls even below the DC current at low fields. The lag, however, is heavily suppressed in devices on the more closely lattice matched sample (A) and enhanced for devices on the structure which is more mismatched (C). Figure 4 shows lag measurements for each of the three devices at many quiescent (gate bias) points. The lag is quantified as the percentage change in the drain current between pulsing from a nonzero quiescent bias voltage on the gate and the baseline.

We believe that the amount of lag is directly related to the number of electrons trapped either on the surface of the semiconductor or within the barrier of the device, acting as a virtual gate [28], not to the amount of leakage current from the Schottky gate metal. Devices with relatively high and low gate leakage on the same sample have reasonably similar degrees of lag; furthermore, devices with similar gate leakage on samples with different barriers have very different degrees of lag. Therefore, the structure of the device is a better predictor of whether a device will exhibit lag than is the gate leakage current. As an example, the gate leakage current density for the devices shown in Fig. 4 at $V_G = -10$ V and $V_D = 7$ V is 44 (A), 72 (B), and 25 μA/mm, (C). Nevertheless, the lag is still somehow related to the gate current for the devices that show moderate to significant amounts of lag (i.e., samples B and C) as illustrated in Fig. 5. Here, the derivative of the gate leakage current (solid lines)

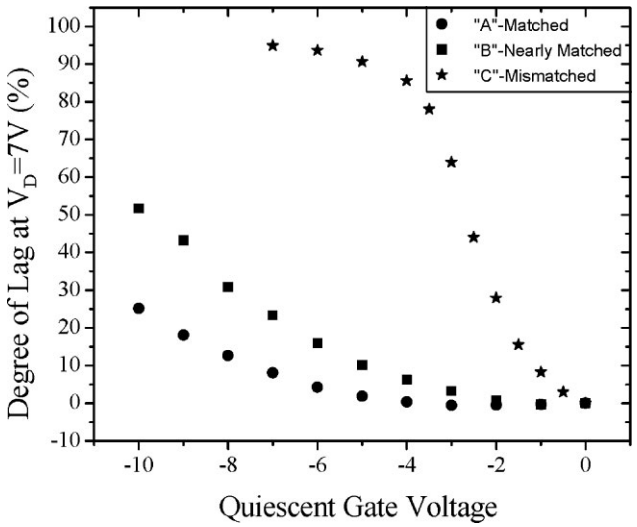

Figure 4 The degree of gate lag as a function of quiescent bias voltage on the gate. Degree of lag is the percent difference between the pulsed value of I_D when pulsing from a quiescent bias voltage on the gate and that at 0 V. The leakage current density for the devices "A", "B", and "C" shown in the figure at $V_G = -10$ V and $V_D = 7$ V is 44 μA/mm, 72 μA/mm, and 25 μA/mm, respectively. Thus, the overall gate leakage is not responsible for observed differences in lag. The pulse lengths are 1 μs and the drain voltage is 7 V.

changes abruptly around the same voltage bias at which the amount of gate lag effect exhibits an increase (symbols). The heavy line and stars represent gate leakage and lag for one device on the lattice mismatched layer while the lighter line and squares represent gate leakage and lag for another

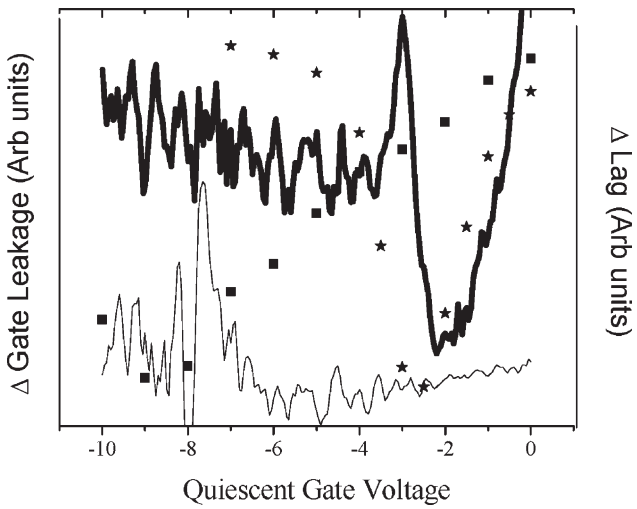

Figure 5 Derivative of gate leakage (lines) and the change in the degree of gate lag (symbols) versus quiescent gate voltage demonstrating the correlation between gate leakage and the gate lag effect for the samples slightly lattice mismatched, "B" (solid line and squares) and lattice mismatched, "C", (heavy solid line and stars) barriers. The drain voltage is measured at 7 V, the pulse width is 1 μs, and the period is 1 ms.

device on the slightly mismatched layer. This may indicate that for some devices, there is a threshold in the gate potential beyond which electrons have access to new leakage paths and subsequent access to traps thereby markedly increasing the gate lag. This would be evidence for the gate lag effect being attributable to electrons that are trapped somewhere in the gate leakage path. However, such a correlation between the derivative of gate current and the amount of lag was not observed for the devices on sample A, which showed very little lag. Further work to elucidate the mechanisms of the gate lag under various bias conditions and at various temperatures is ongoing.

We expect the GaN cap layer to help to mitigate the effect of the gate lag since the lag in the GaN-based HFET structures has been attributed to being a manifestation of slowly moving charges interacting with the polarization charge that resides near the surface [16–19] In fact, nearly dispersion free layers utilizing AlGaN/GaN HFET structures without passivation were reported in Refs [16, 18, 19]. However, in these cases, either the GaN cap layer was much thicker (250 nm) than in our case [16], Si doping of the barrier as well as a 5 nm thick cap layer was employed [18] or some other novel heterostructure was used to avoid the instable charges at the surface [19]. On the contrary, essentially lag-free layers utilizing lattice matched InAlN barrier layers with no such modifications or passivation layers have been reported [14, 15]. We believe that the success of these lattice matched layers is due to the absence of piezoelectric polarization present in the InAlN barrier layer. In order to be manifested as lag, the trapped electrons must respond more slowly to changes in gate potential than the time associated with the lag measurement (1 μsec). Traps whose time constants are faster than the measurement would not contribute to the lag. However, the lag is exacerbated when traps on the surface interact with the dipole charges on the surface associated with (piezoelectric) polarization. In order to be recollected by the gate (and not contribute to the virtual gating and subsequent lag) electrons emitted by the traps must quickly leave the surface. The dipole charges associated with the polarization are an impedance to this movement, thus quickly responding traps may still contribute to lag when they are coupled with these polarization charges. Therefore, layers further from the lattice matched condition exhibit more lag due to the piezoelectric polarization present in those layers. However, we cannot rule out the possibility that samples deviating from the lattice matched condition do not contain more traps, particularly when we consider that relaxation would tend to occur as the composition of the barrier deviates further from the lattice matched condition, and particularly that compressively strained InAlN has been shown to relax even very close to the lattice matched condition [26], which would result in trap generation. In any case, for the samples discussed in this report, we believe that the overall quality of the layers is similar, so the vast differences in gate lag appear to be directly related to the degree of the barrier layers lattice mismatch. As such, we propose the use of the gate lag

measurement as a technique to determine which of a set of layers, with similar crystal quality, is in fact closest to being truly lattice matched.

4 Conclusions In conclusion, we investigated InAlN barrier HFET devices with record high low-temperature mobilities for high density 2DEGs with respectable DC and RF performance. We pointed out the need to accurately determine the residual strain in the underlying GaN layer, in order to determine the appropriate lattice matching condition for InAlN, which is still questionable due to the uncertainty in the values of the lattice parameters of the binaries, as well as the bowing parameters. Nevertheless, in the samples studied in this report, despite changing the values used to determine the composition, we found that the most closely lattice matched sample exhibits the lowest gate lag among all the samples. We also found that while the amount of gate leakage does not correlate with the degree of lag, the derivative of the gate leakage appears to. This would indicate that in devices that show moderate to high degrees of lag, some activated process is at play; new leakage paths become available as potential is increased. These new paths can expose some previously unavailable traps or trap-like states to electrons which can subsequently contribute to gate lag. Our results also indicate that the piezoelectric polarization present in similar compressively strained layers is responsible, in part, for the gate lag since the overall quality of the layers is similar in terms of the Hall mobility and device performance and yet the lag increases as the lattice mismatch increases. Because of this, we propose using the measurement of gate lag as a supplemental technique to ascertain the closeness of comparable layers to the actual lattice matched condition.

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